

## UniPlan™ Hierarchical Floorplanning Technology for Custom Design

As semiconductor-processing technologies move toward smaller geometries, and transistor counts on integrated circuits (ICs) increase significantly every year, the degree of difficulty in completing accurate, full-chip hierarchical floorplanning for custom designs also increases significantly. Accurately estimating chip size, obtaining parasitics early in the design cycle, and meeting chip performance specifications – all while retaining the flexibility required to manage levels of hierarchy and recognize multiple process rules – are critical to meeting tapeout deadlines.

Signal-driven floorplanning, intelligent pin placement and the ability to “push down” into a configurable number of layers of hierarchy are some of the critical custom design automation capabilities that enable the successful on-time completion of custom digital and mixed-signal designs at 45nm and below.

To address these needs, Pulsic UniPlan™ offers a flexible, easy to use – yet comprehensive – hierarchical floorplanning technology bundle for custom physical design. UniPlan centers on a powerful block- and pin-placement engine that complements the skills and knowledge of experienced design floorplanners to create more accurate floor plans that can accommodate major and multiple design changes with ease.

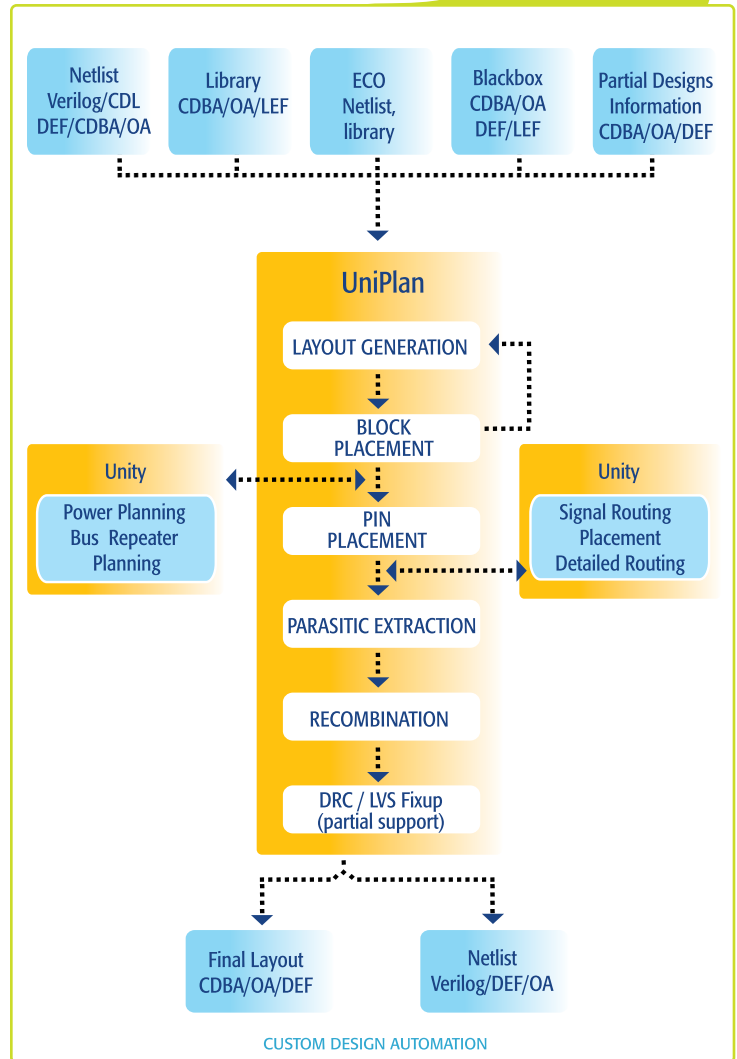
The world’s largest semiconductor companies leverage this technology to achieve faster time to market.

### UNIPLAN - HIERARCHICAL FLOORPLANNING

Pulsic UniPlan is a hierarchical floorplanning technology bundle that provides easy estimation of overall chip size and individual block sizes, top-down or bottom-up floorplanning (with power planning), soft- or hard-block placement, pin placement and legalization, and traversing of the hierarchy.

UniPlan also makes it possible to develop the most flexible floorplans for designs. UniPlan can generate arbitrarily shaped soft blocks that, when placed with the Pulsic UniPlace™ technology, can be reshaped easily for optimum area efficiency, using either standard or variable row height.

#### UniPlan Flow



UniPlan provides rapid feedback after block placement for rectilinear blocks with area and utilization.

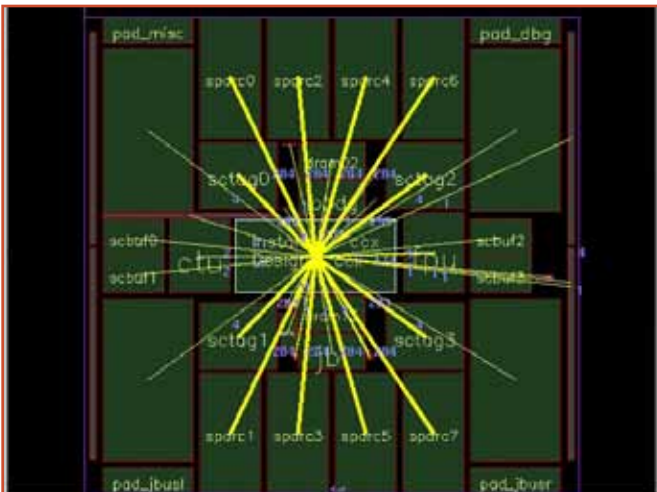
## ▲ CHIP-LEVEL PROTOTYPING

As time-to-market pressures compress design cycles, design leads rarely have time to evaluate multiple floorplans to assess the optimal die size. UniPlan enables designers to explore multiple package configuration options by quickly developing several top-level floorplans using a “black box” or partial-design outline before a netlist is available. Using UniPlan, designers can assess quickly whether or not a design will fit into the allocated area.

Designers can also use UniPlan to perform early congestion analysis by assessing the resources available for top-level pin placement and routing. Designers can use these UniPlan capabilities to extract top-level parasitics and produce a standard parasitics exchange format (SPEF) file for the top-level floorplan, which is critical to the predictability of closure for a design.

## ▲ BLOCK PLACEMENT

The UniPlan block placement engine is a powerful, but highly configurable, placer that places multiple blocks in single- or multiple-block placement areas. It accommodates any rectilinear block shape. UniPlan also supports block clustering, enabling logically connected blocks to be placed adjacent to each other in one area contained within a fence or a guide. As they work with such an area, designers can apply both hard rules, which determine that certain blocks must be placed in a specific area, and soft rules, which specify preferences for blocks to be placed within a specific fence or guide. UniPlan also enables block reuse, so that multiple blocks with similar internal designs can be assembled quickly and easily.



Summary flight lines are illustrated for the floorplan of a cross bar floorplan topology

## ▲ DESIGN PARTITIONING

Today, design teams are often comprised of geographically distributed groups, with a single design undertaken by multiple remote teams. UniPlan enables design leads to partition a design into hierarchical blocks, complete with their associated constraints and design rules. Blocks can be completed by remote teams, and reassembled into the master floorplan when finished.

## ▲ UNIPLAN IN THE UNITY™ PHYSICAL DESIGN SUITE

The UniPlan technology bundle is part of the Pulsic Unity physical design suite. Unity enables designers to generate a layout, create, shape and place blocks, place cells and instances, and route nets within the same environment. Unity integrates the UniPlan floorplanning technology bundle with UniPlace placement technology bundle, and UniRoute™ shape-based routing technology bundle, and UniSignal™ signal integrity and timing technology bundle (including a built-in static-timing analysis engine), enabling design decisions to be implemented in a single environment, without having to move between different tools. As a result, teams can create area-efficient designs rapidly.

## ▲ INTEGRATION WITH INDUSTRY-STANDARD INTERFACES

UniPlan is designed to integrate seamlessly with all industry-standard physical design tools, including the Cadence® Virtuoso® custom design system. UniPlan can export/import directly to/from a Cadence CDBA or OpenAccess database. To enable easy integration with other flows, UniPlan supports industry standards such as LEF/DEF and Verilog® files and imports/exports SDC, SPEF, and .lib formats.

## ▲ HIGH-PERFORMANCE, INTERACTIVE EDITING CAPABILITIES

UniPlan incorporates many powerful interactive and semi-automatic editing features enabled by UniEdit™, the integrated editing technology that is part of the Pulsic Unity physical design suite. UniEdit enables correct-by-construction changes and provides an online design-rule checking (DRC) capability. This comprehensive editing feature included in UniPlan enables layout designers to complete floorplanning operations such as *move block*, *rotate block*, *mirror*, *align*, as well as to edit and reshape blocks, fences, and guides.

## HIERARCHICAL ECO SUPPORT

As designs evolve on an almost daily basis, the engineering change order (ECO) is an inevitable part of any design flow. The Pulsic Unity ECO feature is an integral part of UniPlan, and it provides a comprehensive, automated flow for implementing ECOs in a timely and efficient manner, without impacting the integrity of the design.

## EASE OF USE

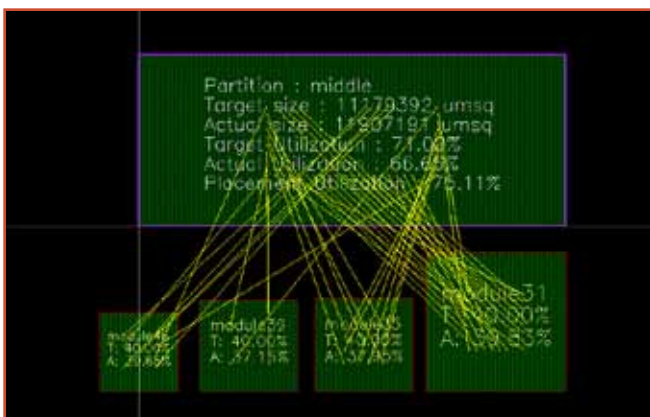
UniPlan is intuitive and easy to use, with an interface that is customizable for specific designs, layout groups, or individual users. The unique Themes™ feature enables designers to customize the UniPlan graphical user interface (GUI) for each set of functions to be performed. Feature buttons, icons, or other options that are required for a specific phase of floorplanning can be visible in the GUI with all other icons and buttons removed to avoid cluttering the desktop with rarely used functions.

UniPlan includes context-sensitive online-help documentation that provides comprehensive feature descriptions with illustrated examples of feature usage and terminology. Comprehensive reporting provides detailed insight at every level of hierarchy.

In addition, UniPlan includes support for the Python scripting language and a Python database API to enable easy batch operations for increased automation of typically manual tasks and optimal utilization of licenses. Configurable bind keys enable seamless operation between UniPlan and other physical design tools.

## ADVANCED NODE SUPPORT

The UniPlan technology bundle has been used successfully by leading fabless and IDM semiconductor companies to complete tapeouts at 45nm and below. With the UniPlan hierarchical support of options and attributes, designers can set rules at the design level, layer level, or at the level of an individual net or class of nets, which is particularly important for advanced process nodes.



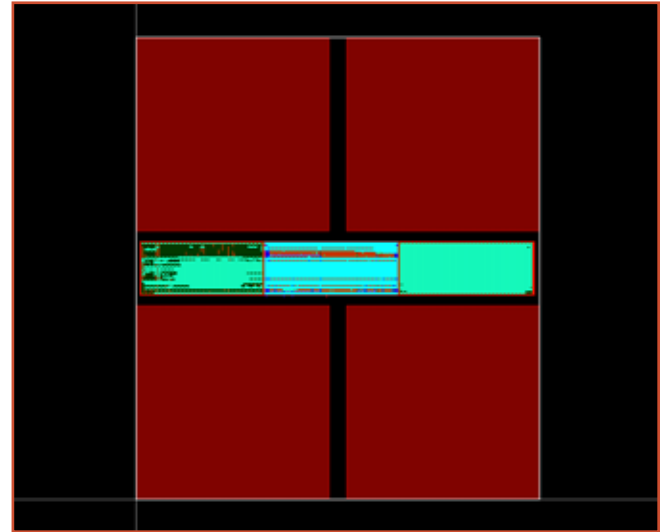
Advance node support enhances adherence to DFM needs

## UNIPLAN TECHNOLOGY FEATURES

- Floorplanning and editing:
  - Flat, hierarchical, and pseudo-hierarchical floorplanning
  - Built-in hierarchy browsing
  - Hierarchical (chip or discrete block) area estimation
  - Automatic soft- and hard-block placement with simultaneous automatic soft-macro shaping
  - Generic (polygonal) soft-macro editing
  - Automatic soft-macro pin optimization and placement
  - Configurable hierarchical constraints from design level to an individual net (or group of nets)
  - Built-in extraction of parasitics for early top-level SPEF generation
  - Powerful interactive editing for block shaping and execution of block-level commands
  - Block unification support
  - Generic (polygonal) floorplan support
- Full power planning:
  - Automation of all power routing through GUI-driven power ring and mesh
  - Power and signal net push-down
- Ease of use:
  - Comprehensive reporting
  - Customizable GUI for streamlined access to specific functions
  - Full scripting of entire flow for batch-mode operation
  - Context-sensitive online Help
- Integration and interfaces:
  - Configurable bind keys for seamless integration with industry-standard flows
  - Tight integration with CDBA/DFII, OpenAccess, LEF/DEF, Verilog, CDL, .lib, DSPF and other timing libraries (input and output)
  - Flexible C++ programming interface and Python® API provide access to components in Pulsic Database (PDB) and enable intelligent and scriptable operations on database

## BENEFITS

- Support for advanced-node process rules for 45nm and below provides silicon-proven confidence of design closure and completion
- True hierarchical floorplanning built for custom design enables predictable closure for leading-edge custom designs
- Simultaneous support of custom-digital and analog environments reduces costs by eliminating the need for separate digital and analog floorplanners
- Can be used as a standalone floorplanning solution, or as part of the Pulsic Unity physical design suite (which includes UniPlace, UniRoute, and UniSignal) for single-environment design implementation
- Operates in conjunction with the Pulsic Unity hierarchical ECO flow to facilitate quick turnaround of incremental ECOs
- Seamless integration with standard design flows and support for both industry- and de facto-standard interfaces and database formats provides the flexibility to use best-in-class UniPlan as part of any EDA flow



*Top level view of hierarchically placed, routed and hardened logic blocks*

## SUPPORT SERVICES

Pulsic provides outstanding support from day one to enable its customers to be productive with UniRoute as quickly as possible.

- Online ticket system allows customers to file their own bug fix and enhancement tickets and monitor progress through email alerts as ticket status is progressed and completed
- Onsite training during evaluation phases enables customers to receive customized training adapted for their own needs
- Implementation support from Pulsic enables users to put UniPlan to work in production flow in minimal time

## PLATFORMS SUPPORTED

- Linux (Red Hat, SUSE), 32-bit, 64-bit
- Sun Solaris (32 bit, 64 bit)



For more information or to schedule a demo, contact your local Pulsic representative

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