

UniRoute™ Shape Based Routing for Extreme Custom Design

The move toward smaller geometries is putting extreme demands on physical semiconductor design tools. The list of “must haves” for today’s routing technologies includes more flexibility, adherence to multiple process rules, and faster performance. The highly specialized nature of custom design automation also makes productivity, yield, area and performance, critical metrics. Consequently, a traditional stand-alone “custom” shape-based router is a minimum requirement for successful on-time completion of custom digital and mixed-signal designs at 45nm and below.

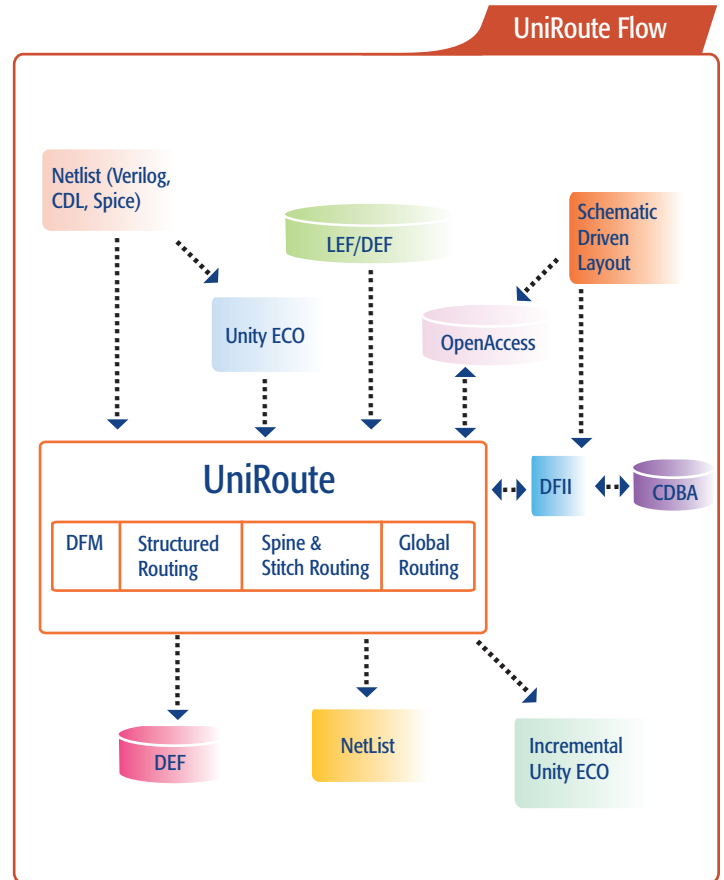
Pulsic addresses this need with a flexible integrated physical design capability. At the center of solution, the Pulsic UniRoute routing engine can complement the skills and knowledge of an experienced layout designer, making it faster and easier to produce high-quality, DRC-correct layout. Alternatively, it can dramatically cut layout time by automating layout, providing the quality of a custom design with the speed of a standard cell design.

The patented UniRoute Spine and Stitch technology delivers a unique channel routing capability that provides the ability to route nets that span long distances in extreme aspect ratio designs. The world’s largest semiconductor companies leverage this technology to achieve faster time to market.

AUTOMATIC ROUTING

Pulsic UniRoute offers custom designers the industry’s most comprehensive, automated shape-based router. Its flexible, highly configurable and easy-to-use shape-based router provides automated and interactive routing for custom digital designs, and specialized analog routing of complex analog circuits. In mixed-signal environments, UniRoute facilitates simultaneous and automated routing of analog and digital nets in the same design, using the same technology, features and database for all design environments.

UniRoute also includes specialized routing functions for extreme aspect ratio designs—such as those found in NAND, NOR, DRAM or other memory layouts. It provides configurable



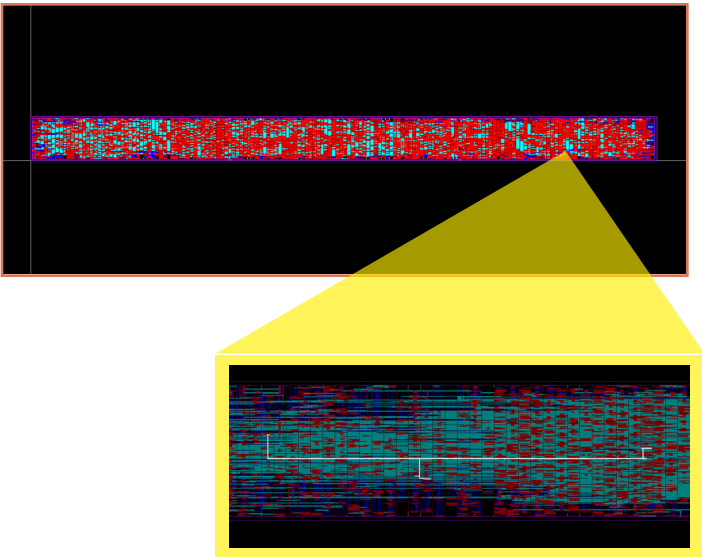
and easily maneuverable bus routing for LCD/LED designs. An interactive and automatic template routing feature enables top-level routing of processors and other complex designs where flexibility and adherence to foundry process rules are critical to design area.

UniRoute is designed to seamlessly integrate with all industry-standard physical design tools, including the Cadence Virtuoso® custom design system. UniRoute can import and export directly to/from a Cadence CDBA or Open Access database. Interfaces with LEF/DEF and Verilog also facilitate easy integration.

SPINE AND STITCH ROUTING

The leading semiconductor companies worldwide use patented UniRoute Spine and Stitch routing to complete the routing of complex, extreme aspect ratio custom designs areas, where area and metals are limited and performance is critical.

The Spine and Stitch router places long 'jogless' spine routes in areas that are heavily congested yet still require every nanometer of space to be used with minimum spacing rules. The unique channel optimization features of UniRoute Spine and Stitch routing allow unused partial routing areas to be "freed up," so that they can be re-used for other routing resources to use that area.

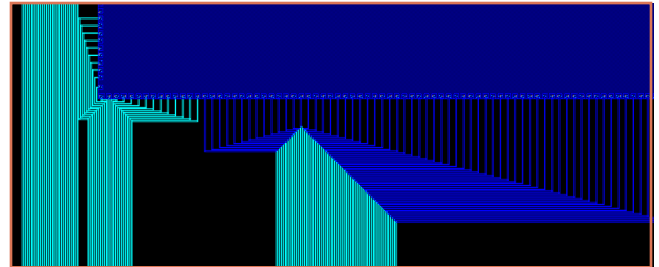


Spine and Stitch Routing increases performance and optimizes area in extreme aspect designs

The UniRoute Spine-and-Stitch router is also used by leaders in the design of logic for NAND, NOR, DRAM, FPGA and LCD/LED applications.

STRUCTURED ROUTING

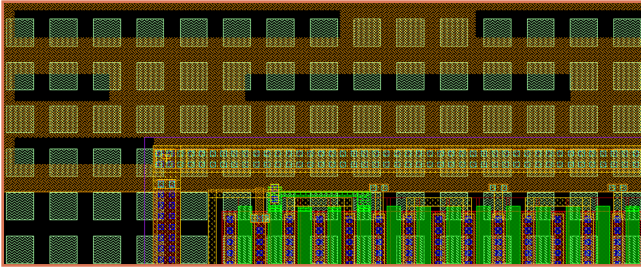
The UniRoute Structured Routing capability provides users with the ability to impose a topology for nets that would otherwise be unstructured. For example, bus routing, power nets and special nets, such as clock nets, can be routed in an orderly and highly configurable pattern to increase performance, and adhere to process rules. Density fill, featuring PowerFill, is a unique capability that allows minimum density fill to be undertaken using power nets. PowerFill allows designers to reinforce power nets by configuring metal fill, area, or percentage of coverage using specific named nets.



Structured Routing includes Bus Routing capability with bus compression to reduce area

ADVANCED NODE SUPPORT

UniRoute has been used by leading fabless and IDM semiconductor companies to successfully complete tapeouts at 40nm and below. Its built-in constraints capabilities encapsulate parallel, wire fattening, dense line ends, and via enclosure rules. And with hierarchical support of options and attributes, rules can be set at the design level, layer level, or down to an individual net or class of nets.



Advance node support enhances adherence to DFM needs

UNEDIT™ – HIGH PERFORMANCE, DRC CORRECT, INTERACTIVE ROUTING

UniRoute incorporates a powerful interactive and semi-automatic editing feature called UniEdit, which is correct by construction and provides an online DRC capability. This feature allows layout designers to complete manual routing operations error-free and DRC-correct every time. The unique 'Push' feature allows wires to be moved while interactively routing, while maintaining the DRC correctness of the layout.

UniEdit includes an 'auto finish' capability so that designers can start routing manually but allow the router to auto finish the route if the optimum route is not easily visible due to congestion. A comprehensive set of editing features also allows users to edit shapes in UniEdit.

FEATURES

- Correct by construction, online DRC correct capability
- Comprehensive shape-based routing capability with successful tapeouts at 65nm (TSMC and IDM), 45nm/40nm (TSMC) and 34nm (IDM)
- Patented Spine and Stitch router provides high-performance jogless routing of nets spanning extreme aspect ratios, and provides layer control and style, or pattern control to designers who are sensitive to functionality and aesthetics
- Hierarchical constraint-driven system enables configurable constraints from design level to individual net (or group of nets)
- Structured routing for all topology, template, and bus routing
- GUI-driven power ring and mesh for automation of power routing generation
- Wire sizing based on current density
- Global router with congestion driven "heat chart"
- Simultaneous observance of optimal spacing and minimum spacing
- System-wide scripting and logging capability enables full scripting of entire flow for batch mode operation
- Comprehensive via support, including:
 - Cadence tech file vias, OpenAccess vias, and all standard LEF/DEF vias
- Range of "analog" routing operations, including slotting, shielding, density fill, net matching, differential pairs, mirror (symmetry) routing, etc.
- Built-in RC extraction
- Density filling, including PowerFill – a highly configurable capability for reinforcing and extending power nets – which is configurable by area and net name
- Powerful interactive routing and editing provides online DRC, correct by construction for interactive or semi-automatic routing operations
- Tightly integrated to CDB/DFII, with support of OpenAccess, LEF/DEF, Verilog, CDL, .lib, DSPF and other timing libraries (input and output)
- Flexible programming C++ interface and python API provides access to components in Pulsic Database (PDB) and allows intelligent and scriptable operations on database

BENEFITS

- Support of advanced node process rules for 45nm and below provides designers with silicon-proven confidence of design closure and completion
- Simultaneous support of custom digital and analog environments reduces costs by circumventing the need for separate tools to route digital and analog nets
- Unique Spine-and-Stitch capability provides superior performance and efficient use of available area for custom designs, especially extreme aspect ratio with highly congested areas that require minimal use of routing area channel optimization avoids using excessive space and aids in die size reduction
- UniRoute is part of the Pulsic Unity™ physical design flow and can be used standalone or as part of a physical design flow with Pulsic UniPlan™ hierarchical floorplanning, UniPlace™ – custom and standard cell autoplacement, UniSignal™ – signal integrity, and Unity Timing – for static timing analysis
- Operates in conjunction with the Pulsic Unity hierarchical ECO flow to facilitate quick turnaround of incremental ECOs
- Seamless integration with other flows and adherence to industry and de facto standard interfaces and databases provides customers with ability to use a best-in-class routing tool integrated with other EDA vendor flows
- Extensive array of enhanced post-routing tools that eliminate the need for other tools for DFM, DFY and other process enhancements



EASE OF USE

- The UniRoute GUI is customizable by users so only the feature buttons required are visible on the toolbar
- Context-sensitive online Help documentation provides comprehensive feature description with illustrated examples of feature usage and terminology
- Configurable Bind keys enables seamless operation between UniRoute and other layout tools
- Python scripting language provides batch usage to optimize use of licensed features and increase total utilization of licenses
- Python Database API capability enables users to manipulate database for automation of functions that are typically undertaken manually

SUPPORT SERVICES

Pulsic provides outstanding support from day one to enable its customers to be productive with UniRoute as quickly as possible.

- Online ticket system allows customers to file their own bug fix and enhancement tickets and monitor progress through email alerts as ticket status is progressed and completed
- Onsite training during evaluation phases enables customers to receive customized training adapted for their own needs
- Implementation support from Pulsic enables users to put UniRoute to work in production flow in minimal time

PLATFORMS SUPPORTED

- Linux (Red Hat, SUSE), 32-bit, 64-bit
- Sun Solaris (32 bit, 64 bit)

For more information or to schedule a demo, contact your local Pulsic representative

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